Joint Online Two Weeks Certificate Program

RISC-V VLSI IMPLEMENTATION FLOW: RTL2GDS

27 March – 9 April, 2021

Jointly Organized by:
IIT Guwahati
NIT Patna
MNIT Jaipur
PDPM IIITDM Jabalpur

Objective & Scope

To enable theoretical and practical understanding of the most popular RISC-V processor implementation from front-end (RTL) to back-end (GDS).

Speakers

- Dr. Aditya Dalakoto, Continental Advanced LiDar Design Solutions
- Puneet Mittal, VLSI Expert Private Ltd

Course Contents

- Simulations and Characterization for Libraries
- Design Basics: Circuit, Architecture and System Level
- Constraints and Synthesis : Input Output Constraints, Complex SoC Constraints.
- Input Output Files : Lib Files, General files needed in complete flow.
- Layer and Power Planning
- Floorplanning
- Delay Calculations and System Implications
- Setup and Hold Discussion
- Placement Basics and Settings
- DRC LVS and Extraction
- Low Power Flow Basics

Joint Principal Coordinators

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Key Features

- Online / Live lectures sessions by subject experts.
- Comprehensive tutorials and practice notes.
- Online lab and training sessions.
- Follow up sessions and discussion forums on research problems and internships.

Course Fee Details

Academic (student/faculty): 500 INR
Industry People : 1000 INR
Others : 1000 INR
Foreign Participants : 4000 INR

Online payment details

Bank Name: Allahabad Bank
Account Name: NIT Patna
Account No.: 50380476798
IFSC Code: IDIB000B810

Link for registration:

https://forms.gle/LW8YESSR3D4Hf1sR9 Last Date for registration : 21.03.2021

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For more details visit:
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