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| **EC5501** | **VLSI Design** | **L-T-P: 3-1-0; Total 42 Lectures** |

***Pre-requisite:*** Basic device electronics, MOSFET properties, and logic circuits.

***Objectives:*** This course is intended to impart in-depth knowledge about analog and digital CMOS circuits. The focus is on CMOS technology. Issues to be covered include deep submicron design, clocking, power dissipation, CAD tools and algorithms, simulation, verification, testing, and design methodology. This course also dealt with design analysis techniques for the static and dynamic evaluation of CMOS circuits and memory elements including flip-flops, SRAM, and DRAM.

***Course Contents:***

**Unit I: Introduction to VLSI design:** Introduction to VLSI Design; Moore’s Law; Scale of Integration; Types of VLSI Chips; Design principles (Digital VLSI); Design Domains(Y-Chart), Challenges of VLSI design- power, timing area, noise, testability reliability, and yield; CAD tools for VLSI design. [6L]

**Unit II: Introduction to VLSI Technology:** VLSI Technology-An Overview-Wafer Processing, Oxidation, Epitaxial Deposition, Ion-implantation and Diffusion; The Silicon Gate Process- Basic CMOS Technology; basic n-well CMOS process, p-well CMOS process; Twin tub process, Silicon on insulator; CMOS process enhancement-Interconnect; circuit elements; 3-D CMOS, SOI, TFET, FINFET. [8L]

**Unit III: Analysis of CMOS logic Circuits:** MOSFET as Switch; Recapitulation of MOS; CMOS Inverter, CMOS logic circuits; NAND gate and NOR Gate; Complex logic circuits; Pass transistor logic; CMOS Transmission gate; CMOS full adder. [10L]

**Unit IV: Advanced Techniques in CMOS logic circuit:** Pseudo nMOS; Tri-state; Clocked CMOS; Dynamic CMOS logic- Domino, NORA, Zipper, etc.; Dual rail logic networks. [8L]

**Unit V: Memories:** Static RAM; SRAM arrays; Dynamic RAMs; ROM arrays; Logic arrays. [5L]

**Unit VI: Testing and Testability:** Motivation for testing, Design for testability, the problems of digital and analog testing, Design for test, Software testing. Faults in Digital Circuits: Controllability, and Observability, Fault models – stuck-at faults, Bridging faults, intermittent faults. Digital Test Pattern Generation: Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D- algorithm, Developments following Roth's D algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Delay fault testing. Testability Techniques: Partitioning and ad-hoc methods and scan-path testing, Boundary scan and IEEE standard 1149.1, Offline built in Self Test (BIST), Hardware description languages and test. [5L]

***Text/Reference Books:***

1. Neil H. E. Weste and Kamran Eshraghian, “Principles of CMOS VLSI Design”, 2nd edition, Pearson Education Asia.
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits: A Design Perspective,” Prentics Hall
3. Sung-Mo Kang, Yusuf Liblebici, “CMOS Digital Integrated Circuits,” Tata Mc Graw HillR. Jacob Baker, “CMOS Mixed-Signal Circuit Design,” Wiley India Pvt. Ltd.
4. Ivan Sutherland, R. Sproull and D. Harris, “Logical Effort: Designing Fast CMOS Circuits”, Morgan Kaufmann

***Course Outcomes:*** After completion of course Student should be able to

1. Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
2. Design MOSFET based logic circuit
3. Draw layout of a given logic circuit
4. Realize logic circuits with different design styles
5. Demonstrate an understanding of working principle of operation of different types of

memories

1. Demonstrate an understanding of working principles of clocking, power reduction and distribution