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| **ECx530** | **Low Power Techniques in VLSI Design** | **L-T-P: 3-0-0; Total 42 Lectures** |

***Pre-requisite****:* Digital Electronics and Digital IC Design

***Objectives:*** Low power Design techniques will be discussed.

***Topics Covered:***

1. Introduction, Sources of Power Dissipation, Static Power Dissipation, the dynamic (switching) power dissipation, short-circuit power dissipation and leakage power dissipation. Low Static/Dynamic Power Techniques, CMOS logic and Pass-Transistor Logic Families (10L)
2. Standard Adder Cells, CMOS Adders Architectures, Parallel Adder. (8L)
3. Types Of Multiplier Architectures, Parallel Multiplier, Braun, Booth and Wallace Tree Multipliers and their performance comparison (10)
4. Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs (6L)
5. Low power VLSI design methodology - LP Physical Design, LP Gate-Level Design, LP Architecture-Level Design, Algorithmic-Level power Reduction. (8L)

***Reading:***

1. J. Rabaey, “Low Power Design Essentials” Springer,2009.
2. KiatSeng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Tata McGraw Hill,2009.
3. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers,2002

**Outcomes:** Upon successful completion of this course, students should be able to:

1. Understand the basics of low power design techniques for battery operated electronic devices.
2. Understand the power dissipation in MOS circuits.
3. Understand the design of low power circuits using static and pass transistor logic.
4. Design different types of adders/multiplier structures.
5. Understand the design of low power CMOS Memories.