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| **ECX511** | **Computer Organization and Architecture** | **L-T-P: 3-0-0; Total 42 Lectures** |

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**Course Objectives:**

The objective of this course is to provide the students the exposure of organization and architecture of MIPS based modern computers and microprocessors. This course attempts to bridge the knowledge gap of the students between the functionality computer hardware and performance of a typical high level language. Further, this course aims to provide brief introduction to the latest topics like cluster computing, GPU, etc.

**Course Outcome:**

Upon completion of the course, students should posse the following knowledge and skills:

* An understanding of a machine's instruction set architecture including basic instruction fetch and execute cycles, instruction formats, control flow, and operand addressing modes.
* The ability to create, assemble, execute, and debug assembly language programs along with a basic understanding of the assembly, linker, and loader processes.
* An understanding of the design and functioning of a machines central processing unit (CPU) including the datapath components and the control unit.
* An understanding of basic input/output functioning including program controlled I/O and interrupt I/O.
* An understanding of organization of memory hierarchies including the basics of cache design.
* Analyze the performance of processors and caches

**UNIT I (3 Lectures)**

Introduction: Performance of a computer; Semiconductor technology and Moore’s Law; Evolution of computer; Function and structure of a computer; Interconnection of components; Performance of a computer; High-level language, assembly language, and machine language.

**UNIT II (6 Lectures)**

Instruction Set: Operations of computer hardware; Operands of computer hardware; Representing instructions in computer; Review of signed/unsigned integers; Binary addition and subtraction, carry and overflow; Logical operations; Decision making; Loop; Sub-routine.

**UNIT III (5 Lectures)**

MIPS Assembly Language Programming: Introduction to operating system; Compiling, assemblining, linking, and loading; The SPIM Simulator; Compilation of C code

**UNIT IV (7 Lectures)**

ALU Design: Addition and subtraction of signed and unsigned integer; Integer multiplication, unsigned and signed multiplication, Booth’s algorithm, sequential multiplier hardware, faster hardware multiplier; Integer division, sequential divide hardware; Integer multiplication and division in MIPS. Floating point representation and IEEE 754 standard, normalized and de-normalized numbers, zero, infinity, NaN; FP comparison, FP addition; Floating point MIPS instructions; Un-optimized and optimized C code for matrix multiplication.

**UNIT V (7 Lectures)**

Designing Processor: Datapath components; Clocking methodology; Designing single-cycle datapath; Control signals and Control unit; Multi-cycle instruction execution; CPI of a multi-cycle processor; Performance comparison of a single-cycle versus a multi-cycle processor; Pipelining versus serial execution; Introduction to MIPS 5-stage pipeline; Pipeline performance; Pipelining hazards; Pipelining vs. instruction level parallelization.

**UNIT VI (7 Lectures)**

Memory Organization: MIPS addressing modes; Main memory organization and performance; SRAM, DRAM, Latency and bandwidth; Memory hierarchy; Cache memory, Virtual memory; Cache memory organization: direct-mapped, fully-associative, and set-associative caches, handling cache miss; Cache performance, memory stall cycles, and average memory access time; Virtual machine.

**UNIT VII (4 Lectures)**

I/O Organization: Accessing of I/O devices; Interrupts; Direct memory access; Buses; Interface circuits; Standard I/O interfaces (PCI, SCSI, USB).

**UNIT VIII (3 Lectures)**

Advanced Topics: Difficulty of creating parallel processing programs; Parallelism - Multicores, Clusters, Graphics Processors (GPUs); Flynn classification; RAID configuration of hard disks

**Text Books:**

1. Computer Organization and Design: The Hardware Software Interface, David Patterson and John Hennessy, Morgan Kufmann, 5th Edition.
2. Computer System Architecture, Morris Mano, Prentice-Hall India, Eastern Economy Edition.

**Reference Books:**

1. Computer Architecture and Organization, John P Hayes, McGraw-Hill International Editions, Computer Science Series.
2. Computer Organization, Carl Hamacher, Zvonko Vranesic & Safwat Zaky, Mc Graw Hill.
3. Computer Organization and Architecture, William Stallings, Pearson Education.
4. Aho, A., R. Sethi, and J. Ullman [1985]. Compilers: Principles, Techniques, and Tools, Reading, MA: Addison-Wesley.
5. Sweetman, D. [1999]. See MIPS Run, San Francisco, CA: Morgan Kaufmann Publishers.