|  |  |
| --- | --- |
| MONO | **DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**  **NATIONAL INSTITUTE OF TECHNOLOGY PATNA**  Ashok Raj Path, PATNA 800 005 (Bihar), India |
| Phone No.: 0612 – 2372715, 2370419, 2370843, 2371929, 2371930, 2371715 Fax – 0612- 2670631 Website: [www.nitp.ac.in](http://www.nitp.ac.in/) |

## CS4401 Computer Architecture

**L-T-P-Cr: 3-0-0-3**

**Pre-requisites** – Introduction to Computing, Data Structures, Digital Logic and Circuits.

**Objectives/Overview:**

* To cover fundamental concepts of computer architecture and computer organization (particularly, structures and functions of significant components of computer systems)
* To know their design/functioning perspectives.
* To relate these concepts to contemporary design of computer systems.

**Course Outcomes** – After completing this course, students should be able to:

1. *recall* theories about structural and functional aspects of computer systems and their components;
2. *cite* elementary/advanced design principles of computer system components, with suitable examples of early and contemporary CISC and RISC systems;
3. *indicate* organizational and architectural perspectives in different design aspects of computer systems;
4. *apply* architectural and organizational features of computer system components conforming to their design requirements;
5. *solve* qualitative and quantitative problems on design principles of sequential as well as parallel processing systems using appropriate methods.
6. *determine* performance complexities of sequential and parallel processing systems in solving practical problems.

**Course Outcomes–Cognitive Levels–Program Outcomes Matrix –  
[S: Strong relation (3); M: Moderate relation (2); W: Weak relation (1); N: No relation (0)]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course Outcomes** | **Cognitive Levels** | **Program Outcomes** | | | | | | | | | | | |
| PO-1 (Engineering knowledge) | PO-2 (Problem analysis) | PO-3 (Design/development of solutions) | PO-4 (Conduct investigations of complex problems) | PO-5 (Modern tool usage) | PO-6 (The engineer and society) | PO-7 (Environment and sustainability) | PO-8 (Ethics) | PO-9 (Individual and team work) | PO-10 (Communication) | PO-11 (Project management and finance) | PO-12 (Life-long learning) |
| CO-1 | Knowledge | S | S | S | W | W | W | M | W | M | S | W | S |
| CO-2 | Knowledge | S | S | S | M | W | M | S | M | M | S | W | S |
| CO-3 | Comprehension | S | S | S | M | W | W | S | M | M | S | W | S |
| CO-4 | Application | S | S | S | M | M | M | S | S | M | S | M | S |
| CO-5 | Application | S | S | S | S | S | M | M | S | M | S | M | S |
| CO-6 | Analysis | S | S | S | S | S | M | S | S | M | S | M | S |

**UNIT I: Lectures: 18**

**Introduction:** Introduction to computer organization and architecture; Structural and functional views of computer system; ALU and data path.

**Computer Arithmetic & ALU:** Computer arithmetic; ALU data path design for integer addition, subtraction, multiplication and division; Fixed-point and floating-point representations; FPU data path design for floating-point addition, subtraction, multiplication and division; Guard, round and sticky bits in FPU.

**Instruction Set Architecture:** Instruction set; CISC and RISC systems; Instruction cycle and state diagram; Instruction set design factors: instruction types, data types, instruction formats, register organizations, addressing modes; Instruction sets in CISC and RISC systems.

**Microprogrammed Control:** Control unit design: hardwired, microprogrammed approaches; Microinstruction sequencing; Control memory; Control unit in CISC and RISC systems.

**UNIT II: Lectures: 12**

**Memory System:** Memory system characteristics and design objectives; Memory hierarchy in CISC and RISC systems; Cache memory principle and organization; Cache memory mapping; Cache replacement algorithms; Cache writing policies; Unified and split caches; Random access memory; External memory: disk-based storage and RAIDs, optical storage, SSD storage; Virtual memory, paging and segmentation.

**Input/Output Organization:** I/O structures and functions; I/O techniques: programmed I/O, interrupt-driven I/O, DMA; Interrupt and interrupt controller; Bus arbitration.

**UNIT III: Lectures: 12**

**Pipelining and Parallelism:** Nature of parallelism in computer systems; Instruction-level parallelism; RAW, WAW, WAR dependencies; Instruction pipelining; Pipelining hazards; Branch prediction; Superscalar pipelining; Instruction issue policy; Pipelines in CISC and RISC systems; Processing system classification.

**Parallel Processing:** Data parallelism; Vector processing; Multithreading in CPU; Shared-memory multiprocessors; SMP cache coherence: directory, snoopy, MESI protocols; NUMA and CC-NUMA systems; Multicore systems; Distributed-memory multiprocessor systems; Multicomputer systems; Clusters; MPPs; Case studies of parallel processing systems.

**Text/ Reference Book(s):**

1. William Stallings, *Computer Organization and Architecture: Designing for Performance*, Pearson Education, Tenth edition, 2016.
2. Andrew S. Tanenbaum, Todd Austin, *Structured Computer Organization*, Pearson Education, Sixth edition, 2013.
3. John L. Hennessy, David A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann, Sixth edition, 2017.
4. David A. Patterson, John L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, Morgan Kaufmann, Fifth edition, 2014.
5. Sarah L. Harris, David M. Harris, *Digital Design and Computer Architecture: ARM® Edition*, Morgan Kaufmann, 2016.
6. Barry B. Brey, *The Intel Microprocessors: Architecture, Programming, and Interfacing*, Pearson Education, Eighth edition, 2009.
7. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian, *Computer Organization and Embedded Systems*, McGraw-Hill, Sixth edition, 2011.
8. Hesham El-Rewini, Mostafa Abd-El-Barr, *Advanced Computer Architecture and Parallel Processing*, John Wiley & Sons, 2005.